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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: **DONALD E. DEMMING, ET AL.**	§	Docket No. **TU9-98-010**
Serial No. **09/131,846**	§	Examiner: **BRYCE P. BONZO**
Filed: **July 24, 1998**	§	Art Unit: **2184**
For: **DATA PROCESSING METHOD AND SYSTEM FOR SIMULATION OF HARDWARE FAULTS UTILIZING A PCI BUS**	§	

APPEAL BRIEF UNDER 37 C.F.R. §1.192

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

This Brief is submitted in triplicate in support of the Appeal in the above-identified patent application.

CERTIFICATE OF MAILING
37 CFR § 1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Assistant Commissioner of Patents, Washington, D. C. 20231 on the date below.

9/18/2001
Date

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REAL PARTY IN INTEREST

The real party in interest in the present Appeal is International Business Machines Corporation (*IBM*), the Assignee of the present Application as evidenced by the Assignment set forth at Reel 9383, Frame 0621.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant, the Appellant's legal representative, or assignee, which directly affect or would be directly affected by or have a bearing on the Board's decision in the pending appeal.

STATUS OF CLAIMS

Claims 1-18 stand finally rejected as noted in the Advisory Action dated May 22, 2001.

STATUS OF AMENDMENT

No Amendment has been submitted subsequent to the Final Rejection in the present Application.

SUMMARY OF INVENTION

The present invention describes a method and system for simulating a hardware fault occurring on an expansion card coupled to a data processing system utilizing a bus. A fault simulator card 18 is illustrated in Figure 2 and described in the present Specification at page 7, line 9, *et seq*. As depicted, fault simulator 18 includes a Digital-to-Analog Converter 30 (DAC), a buffer amplifier 32, a control register 34, multiple relays 36 and multiple relays 37.

DAC 30 and control register 34 both receive as their inputs a control signal 41 which is output by decoder 39. Decoder 39 receives, utilizing PCI box 24, and decodes a signal 38

from processing unit 12. Control signal 41 includes information regarding which line or lines of PCI bus are to be utilized to test the response of processing unit 12 to a particular hardware fault. Control signal 41 also includes information regarding the test voltage level to be utilized during the simulation.

DAC 30 is then utilized to convert the digital information regarding the test voltage level to the proper analog voltage level. DAC 30 outputs an analog signal 40 having a first voltage level to buffer amplifier 32 which amplifies signal 40 and outputs it as test voltage signal 42. Any number of different test voltage levels can therefore be selected and generated utilizing DAC 30 and buffer amplifier 32. Test voltage signal 42 is then received by multiple relays 36.

Control register 34 also receives information regarding which line or lines of PCI bus 24 are to be utilized to test the response of processing unit 12 to a particular hardware fault. Control register 34 is utilized to turn selected relays 36 and 37 either on or off. Control register 34 is coupled to relay 36a via signal 48, relay 36b via signal 46, relay 36c via signal 44, relay 37a via signal 50, relay 37b via signal 52, and relay 37c via signal 54. Control register 34 includes a bit associated with each signal output from control register 34 which may be either set or reset to drive the signal either HIGH or LOW.

As an example, when a particular hardware fault calls for PCI line 56 to be driven HIGH, control signal 41 includes information which sets a bit in control register 34 associated with signal 48 to drive signal 48 HIGH, and resets a bit in control register 34 associated with signal 50 to drive signal 50 LOW. Relay 36a is turned on while relay 37a is turned off. This causes the test voltage signal 42 to be output on PCI line 56, thus simulating the selected hardware fault at a particular voltage level.

ISSUE ON APPEAL

1. Is the Examiner's rejection of Claims 1-18 under 35 U.S.C. §102(e) as being anticipated by *Gates,* U.S. Patent No. 5,701,409 well founded?

GROUPING OF CLAIMS

For purposes of this Appeal Claims 1-18 stand or fall together as a single group.

ARGUMENT

Gates discloses an integrated circuit which includes a bus error generation circuit coupled to a bus interface terminal of the integrated circuit. After a particular error command is loaded into the command register of the bus error generation circuit of *Gates*, an incorrect parity value is output onto the PCI bus terminal during a subsequent data write PCI bus cycle. A target device on the PCI bus then receives that data and the incorrect parity, logs the error condition by setting a bit in its status configuration register, and asserts the parity error signal on PERR# line back to the initiator device. Upon receiving the parity error signal on the PERR# line, the master device sets an appropriate bit in its status configuration register. The command register of the bus error generation circuit is cleared so that the error condition will be generated only once. In this manner *Gates* teaches that the device on the PCI bus which loaded the master device with the error command can read the status configuration registers of the master and target devices over the PCI bus to make sure that the incorrect parity value on the PCI bus was properly detected and handled on the PCI bus.

Figure 9A of *Gates* illustrates the various digital commands which can be generated utilizing the parity error generator of that disclosure.

In direct and utter contrast to the teaching of *Gates*, the circuit depicted in Figure 2 of the present Application includes a digital-to-analog converter 30 which generates "an analog voltage signal representative of said specified hardware fault . . ." which is thereafter output during operation of the expansion card in accordance with each of the claims of the present Application. Applicant has urged the Examiner to consider that as each of the claims in the present Application expressly recites the utilization of analog voltages, that the citation of the *Gates* reference is improper. The Examiner has dismissed this argument noting a belief that "all voltage in common practice is analog."

Applicant respectfully disagrees and notes that "digital" and "analog" are specific terms of art which have specific and definite meaning within the electronics art which may not be altered by the Examiner in an effort to apply a prior art reference which is clearly inapplicable.

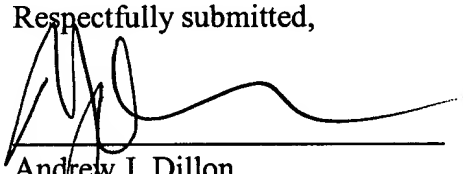
As set forth within the Microsoft Press Computer Dictionary, Third Edition, "analog" is defined as "pertaining to or being a device or signal having the property of continuously varying in strength or quantity, such as voltage or audio" in clear and direct contrast, "digital" is defined within the aforementioned Microsoft Press Computer Dictionary, as "in computing, analogous to binary because the computer is familiar to most people process information coded as combination of binary digits."

Further, even assuming for *arguendo* that all voltage is analog, nothing within *Gates* shows or suggests in any way the creation of an analog signal which is "representative of said specific hardware fault" as set forth within the claims of the present Application. The mere presence of the voltage level within *Gates* which does not constitute a logical "one" or "zero" fails to anticipate, show or suggest in any way the creation of an analog voltage signal which is representative of the specified hardware fault as expressly required by the present claims.

In view of the above, Applicant urges that the Examiner's rejection of Claims 1-18 under 35 U.S.C. §102(e) as being anticipated by *Gates* is not well founded and reversal of that rejection is respectfully requested.

Please charge IBM Corporation Deposit Account No. **09-0449** in the amount of $310.00 for submission of a Brief in support of an Appeal. No additional fees or expenses are believed to be required; however, if any additional fees are required, please charge IBM Corporation Deposit Account No. **09-0449**.

Respectfully submitted,



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ATTORNEY FOR APPLICANT

APPENDIX

1. A method in a data processing system for simulating a hardware fault occurring on an expansion card, said expansion card coupled to a processing unit in said system utilizing a bus, said method comprising the steps of:

specifying said hardware fault to simulate;

determining a signal to output utilizing said bus to simulate said hardware fault occurring on said expansion card;

creating an analog voltage signal representative of said specified hardware fault; and

outputting said analog voltage signal during operation of said expansion card ,wherein said hardware fault occurring on said expansion card is simulated.

2. The method according to claim 1, wherein said step of determining a signal to output utilizing said bus to simulate said hardware fault occurring on said expansion card further comprises the step of determining a signal to output utilizing a PCI bus to simulate said hardware fault occurring on said expansion card.

3. The method according to claim 1, further comprising the step of prior to outputting said analog voltage signal, determining a proper response of said system to said hardware fault.

4. The method according to claim 3, further comprising the step of in response to outputting said analog voltage signal, determining if said system responded properly to said hardware fault.

5. The method according to claim 4, further comprising the step of determining a line of said bus which is associated with said hardware fault.

6. The method according to claim 5, further comprising the step of outputting said analog voltage signal during operation of said expansion card utilizing said line of said bus.

7. The method according to claim 6, further comprising the step of determining a test voltage level for said analog voltage signal, wherein said test voltage level is a voltage level required to simulate said hardware fault.

8. The method according to claim 7, further comprising the step of outputting said analog voltage signal having said test voltage level during operation of said expansion card utilizing said line of said bus.

9. The method according to claim 8, wherein said step of determining a signal to output utilizing said bus to simulate said hardware fault occurring on said expansion card further comprises the step of determining a signal to output utilizing a PCI bus to simulate said hardware fault occurring on said expansion card.

10. A data processing system for simulating a hardware fault occurring on an expansion card, said expansion card coupled to a processing unit in said system utilizing a bus, comprising:

means for specifying said hardware fault to simulate;

means for determining a signal to output utilizing said bus to simulate said hardware fault occurring on said expansion card;

means for creating an analog voltage signal representative of said specified hardware fault; and

means for outputting said analog voltage signal during operation of said expansion card, wherein said hardware fault occurring on said expansion card is simulated.

11. The method according to claim 10, wherein said means for determining a signal to output utilizing said bus to simulate said hardware fault occurring on said expansion card further comprises means for determining a signal to output utilizing a PCI bus to simulate said hardware fault occurring on said expansion card.

12. The system according to claim 10, further comprising means prior to outputting said analog voltage signal, for determining a proper response of said system to said hardware fault.

13. The system according to claim 12, further comprising means responsive to outputting said analog voltage signal, for determining if said system responded properly to said hardware fault.

14. The system according to claim 13, further comprising means for determining a line of said bus which is associated with said hardware fault.

15. The system according to claim 14, further comprising means for outputting said analog voltage signal during operation of said expansion card utilizing said line of said bus.

16. The system according to claim 15, further comprising means for determining a test voltage level for said analog voltage signal, wherein said test voltage level is a voltage level required to simulate said hardware fault.

17. The system according to claim 16, further comprising means for outputting said analog voltage signal having said test voltage level during operation of said expansion card utilizing said line of said bus.

18. The system according to claim 17, wherein said means for determining a signal to output utilizing said bus to simulate said hardware fault occurring on said expansion card further comprises means for determining a signal to output utilizing a PCI bus to simulate said hardware fault occurring on said expansion card.

Microsoft Press
Computer Dictionary

Third Edition

Microsoft Press

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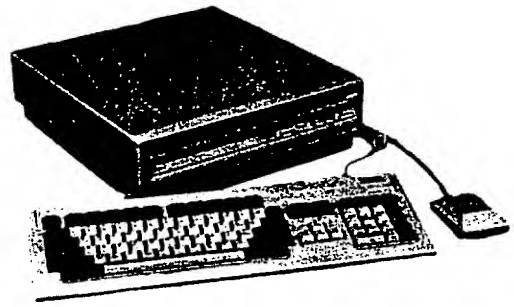
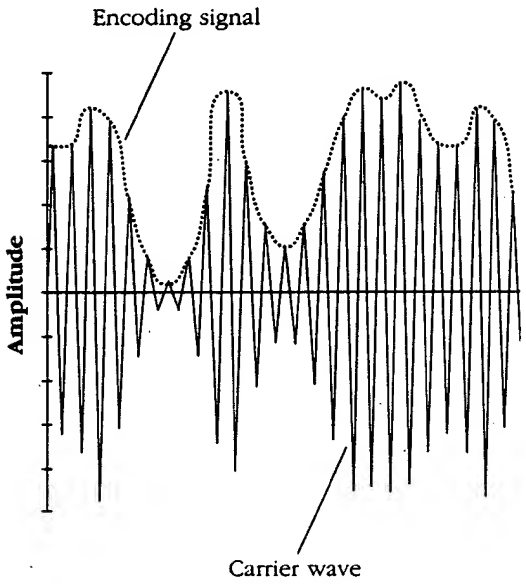


Amiga.

amplitude \am´plə-to͞od`\ *n.* A measure of the strength of a signal, such as sound or voltage, determined by the distance from the baseline to the peak of the waveform. *See also* waveform.

amplitude modulation \am`plə-to͞od moj-ə-lā´-shən, mod-yə-lā´shən\ *n.* A method of encoding information in a transmission, such as radio, using a carrier wave of constant frequency but of varying amplitude. See the illustration. *Acronym:* AM (A´M).

AMPS \A`M-P-S´\ *n.* Acronym for **A**dvanced **M**obile **P**hone **S**ervice. One of the original cellular phone services, relying on frequency-division multiplexing.



Amplitude modulation.

AMPS/NAMPS \amps`N´amps, A-M-P-S`N´A-M-P-S`\ *n. See* AMPS, NAMPS.

AMT \A`M-T´\ *n. See* address mapping table.

.an \dot`A-N´\ *n.* On the Internet, the major geographic domain specifying that an address is located in the Netherlands Antilles.

analog \an´ə-log`\ *adj.* Pertaining to or being a device or signal having the property of continuously varying in strength or quantity, such as voltage or audio. *Compare* digital (definition 2).

analog channel \an´ə-log chan`əl\ *n.* A communications channel, such as a voice-grade telephone line, carrying signals that vary continuously and can assume any value within a specified range.

analog computer \an`ə-log kəm-pyo͞o´tər\ *n.* A computer that measures data varying continuously in value, such as speed or temperature.

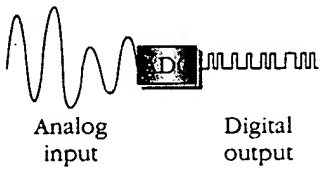
analog data \an´ə-log dā`tə, dat`ə\ *n.* Data that is represented by continuous variations in some physical property, such as voltage, frequency, or pressure. *Compare* digital data transmission.

analog display \an´ə-log dis-plā`\ *n.* A video display capable of depicting a continuous range of colors or shades rather than discrete values. *Compare* digital display.

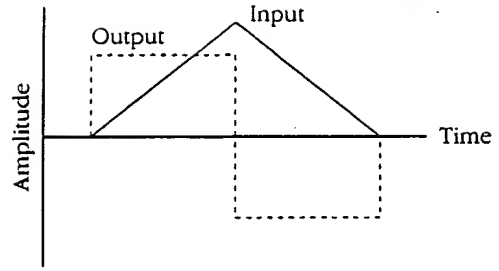
analog line \an´ə-log līn`\ *n.* A communications line, such as a standard telephone line, that carries continuously varying signals.

analog signal generator \an`ə-log sig-nəl jen´ər-ā-tər\ *n.* A device that generates continuously variable signals and is sometimes used to activate an actuator in a disk drive. *See also* actuator.

analog-to-digital converter \an`ə-log-tə-dij`i-təl kən-vər´tər\ *n.* A device that converts a continuously varying (analog) signal, such as sound or voltage, from a monitoring instrument to binary code for use by a computer. See the illustration. *Acronym:* ADC (A`D-C´). *Also called* A-D converter. *See also* modem. *Compare* digital-to-analog converter.



Analog-to-digital converter.



Differentiator. An example of the action of a differentiator circuit.

subscribers in place of the multiple individual posts that the digest contains. If the mailing list is moderated, the digest may be edited. *See also* moderated.

digicash \dij'ikash'\ *n. See* e-money.

digit \dij'it\ *n.* One of the characters used to indicate a whole number (unit) in a numbering system. In any numbering system, the number of possible digits is equal to the base, or radix, used. For example, the decimal (base-10) system has 10 digits, 0 through 9; the binary (base-2) system has 2 digits, 0 and 1; and the hexadecimal (base-16) system has 16 digits, 0 through 9 and A through F.

digital \dij'i-təl'\ *adj.* **1.** Related to digits or the way they are represented. **2.** In computing, analogous to *binary* because the computers familiar to most people process information coded as combinations of binary digits (bits). *Compare* analog.

digital audio disc \dij'i-təl ä'dē-ō disk', ô'dē-ō\ *n. See* compact disc.

digital audio tape \dij'i-təl ä'dē-ō tāp, ô'dē-ō tāp\ *n.* A magnetic tape storage medium for recording digitally encoded audio information. *Acronym:* DAT (dat, D'A-T').

digital audio/video connector \dij'i-təl ä'dē-ō-vid'ē-ō kə-nek'tər, ô'dē-ō\ *n.* An interface on some high-end video cards or TV tuner cards that allows the simultaneous transmission of digital audio and video signals. *Also called* DAV connector. *See also* interface (definition 3), video adapter.

digital camera \dij'i-təl kam'ər-ə, kam'rə\ *n.* A type of camera that stores photographed images electronically instead of on traditional film. A digital camera uses a CCD (charge-coupled device) element to capture the image through the lens when the operator releases the shutter in the camera; circuitry within the camera then stores the image captured by the CCD in a storage medium such as solid-state memory or a hard disk. After the image has been captured, it is downloaded by cable to the computer using software supplied with the camera. Once stored in the computer, the image can be manipulated and processed much like the image from a scanner or related input device. *See also* charge-coupled device.

digital cash \dij-i-təl kash'\ *n. See* e-money.

digital communications \dij'i-təl kə-myōō-nə-kā'shənz\ *n.* Exchange of communications in which all information is transmitted in binary-encoded (digital) form.

digital computer \dij'i-təl kəm-pyōō'tər\ *n.* A computer in which operations are based on two or more discrete states. Binary digital computers are based on two states, logical "on" and "off," represented by two voltage levels, arrangements of which are used to represent all types of information—numbers, letters, graphics symbols, and program instructions. Within such a computer, the states of various circuit components change continuously to move, operate on, and save this information. *Compare* analog computer.

Digital Darkroom \dij'i-təl därk'rōōm\ *n.* A Macintosh program developed by Silicon Beach Software for enhancement of black-and-white photographs or scanned images.

digital data transmission \dij'i-təl dā'tə tranz-mish'ən, dat'ə\ *n.* The transfer of information encoded as a series of bits rather than as a fluctuating (analog) signal in a communications channel.

digital display \dij'i-təl dis-plā'\ *n.* A video display capable of rendering only a fixed number of colors or gray shades. Examples of digital displays are IBM's Monochrome Display, Color/Graphics Display, and Enhanced Color Display. *See also* CGA, EGA, MDA. *Compare* analog display.

digital line \dij'i-təl līn'\ *n.* A communications line that carries information only in binary-encoded (digital) form. To minimize distortion and noise interference, a digital line uses repeaters to regenerate the signal periodically during transmission. *See also* repeater. *Compare* analog line.